New Digital Low Level RF for Elettra Storage Ring

Paolo Pittana, Luca Zanella,
Mauro Bocciai, Mauro Rinaldi, Mitja Gustin

Summary

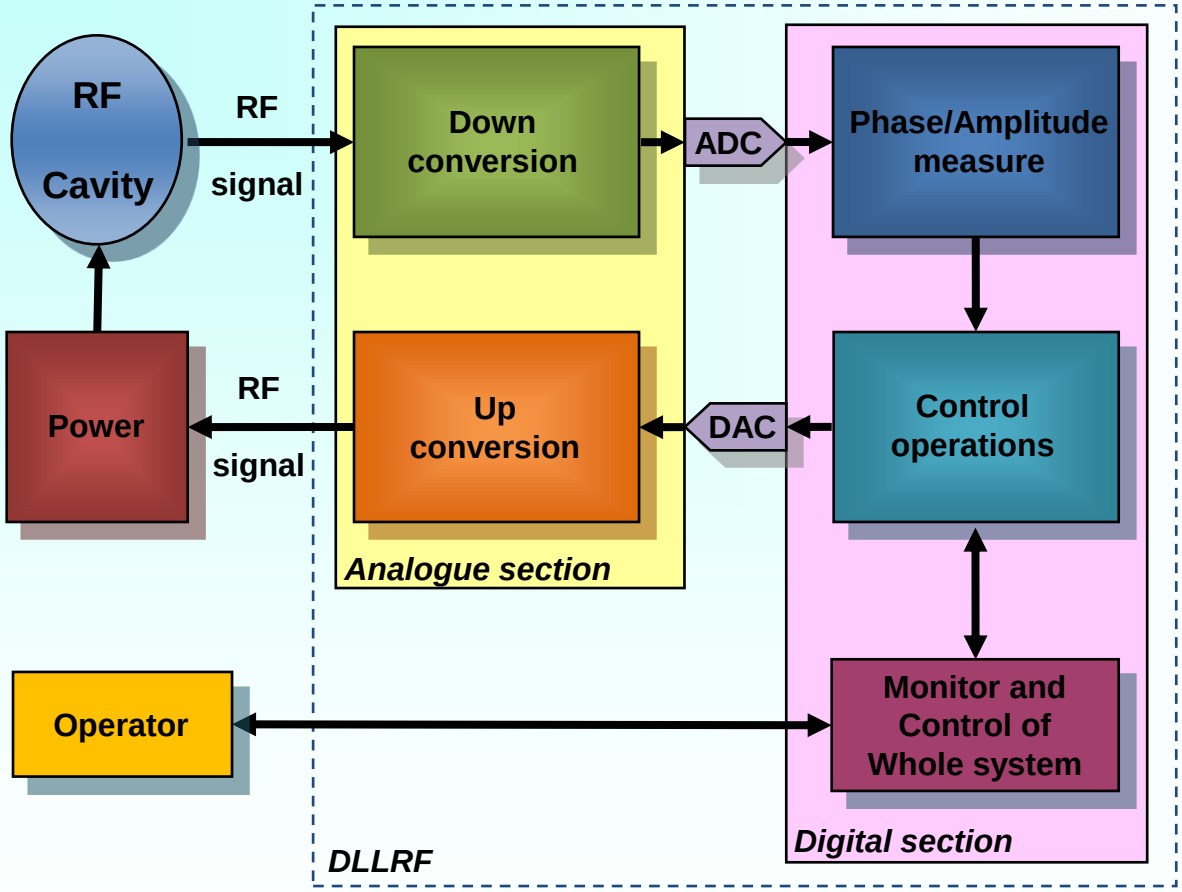
- *Technical requirements*
- *General Architecture*
- *Down Conversion section*
- *Converters and Modulator*
- *Digital Section*
- *Final Considerations*

Technical requirements

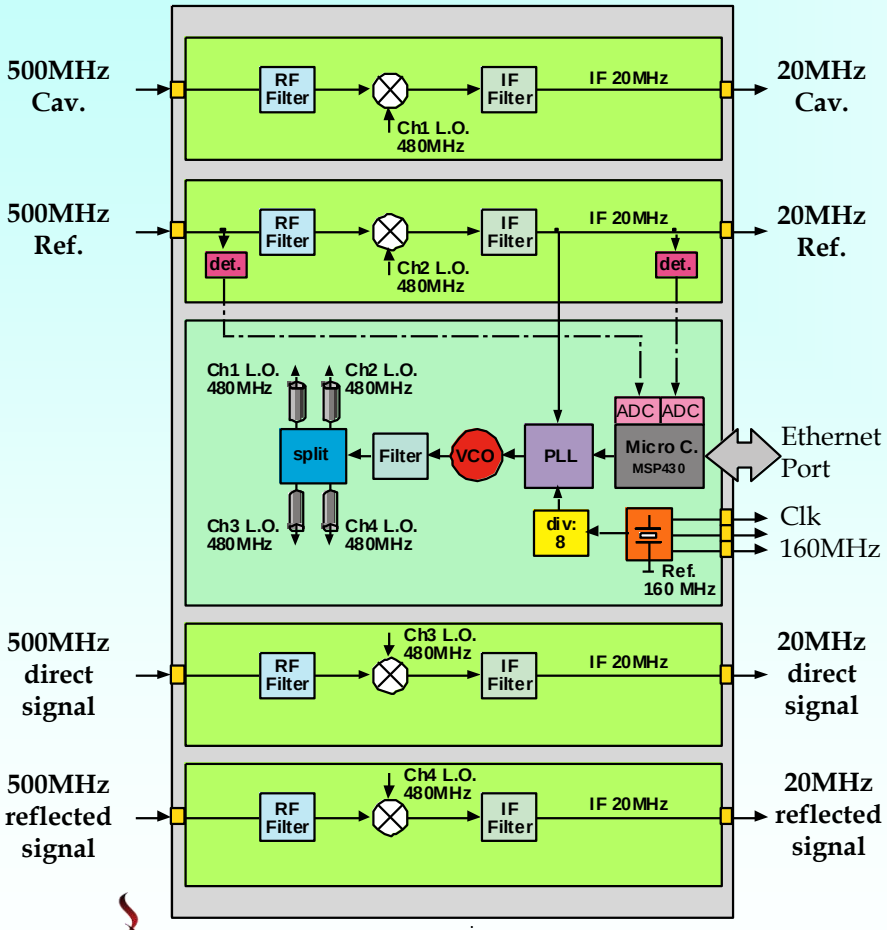
- *Elettra LLRF: present and future performances*
  - *RF input frequency 500MHz*
  - *Amplitude control @maximum power operation: 0,2%* *(now: 2%)*
  - *Phase control @maximum power operation : 0,1°* *(now: 1°)*
  - *Compatibility with old system*

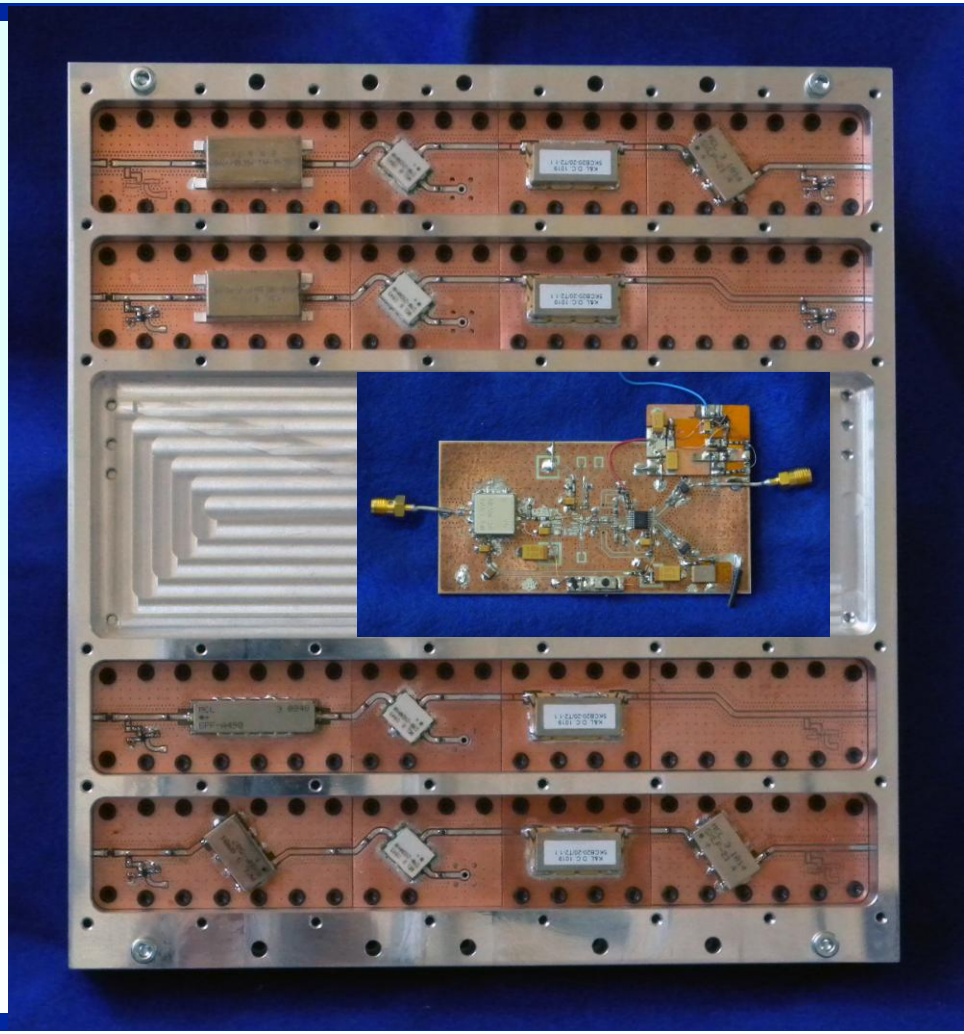
- *…Further important requirement for the DLLRF:*
  - *"Adaptable" Down Conversion Section, in order to be compatible with different RF systems*

General Architecture

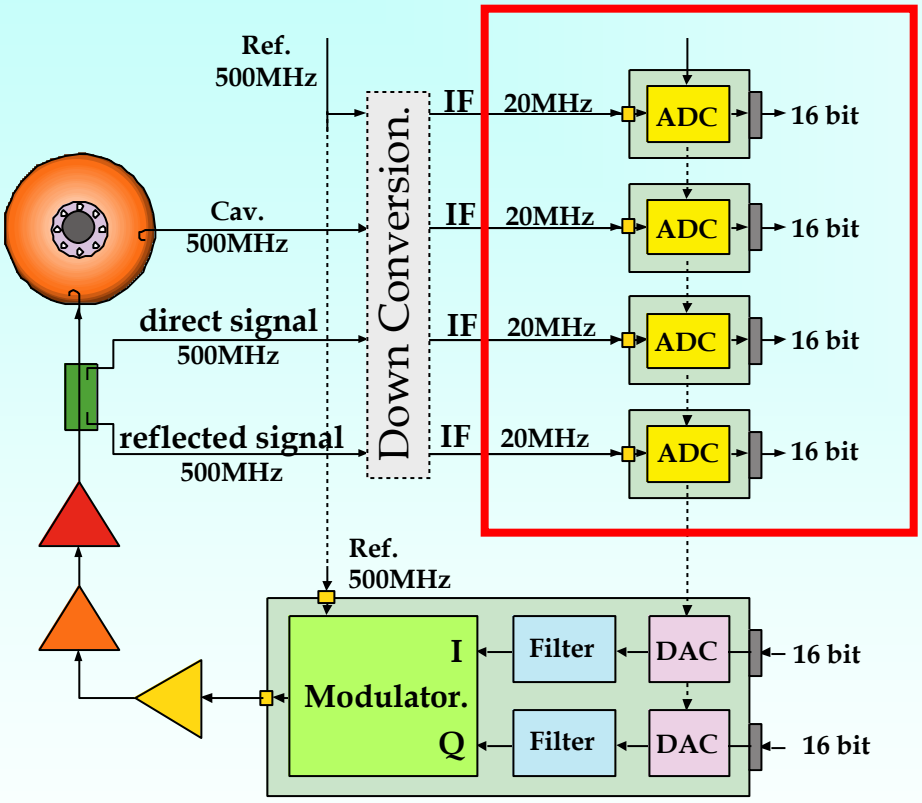


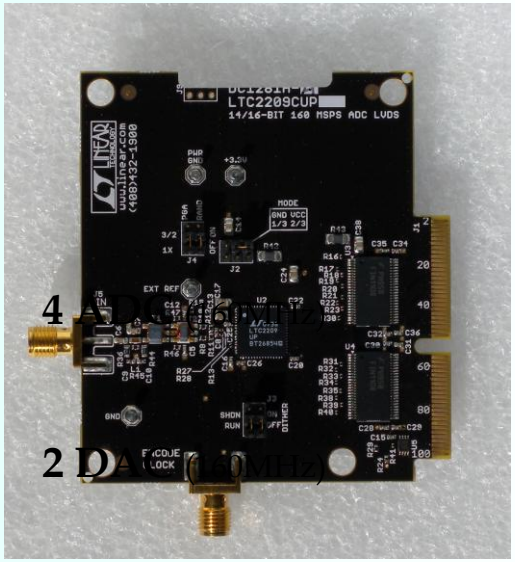
Down Conversion Section





Converters and Modulator - 1





4 ADC (160MHz)

2 DAC (160MHz)

1 Vectorial modulator (500MHz)

Phase Resolution ±0.1 deg ⇨ 11bit

Amplitude Resolution ±0.1 % ⇨ 11bit

8 samples for cycle IF 20MHz ⇨ Clk = 160MS/s

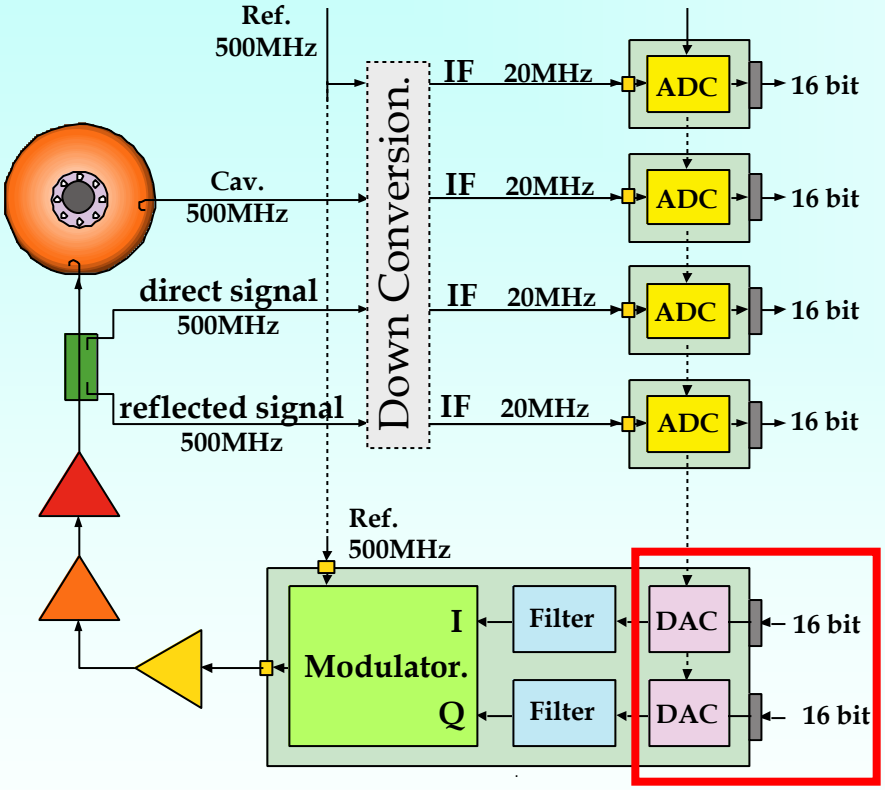
ADC: LTC2209

160MS/s

16 nominal bit

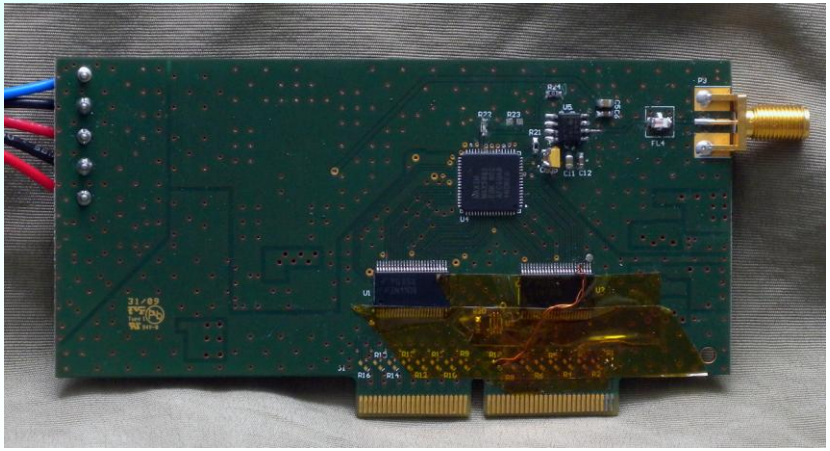
ENOB = 12.5bit

Converters and Modulator - 2

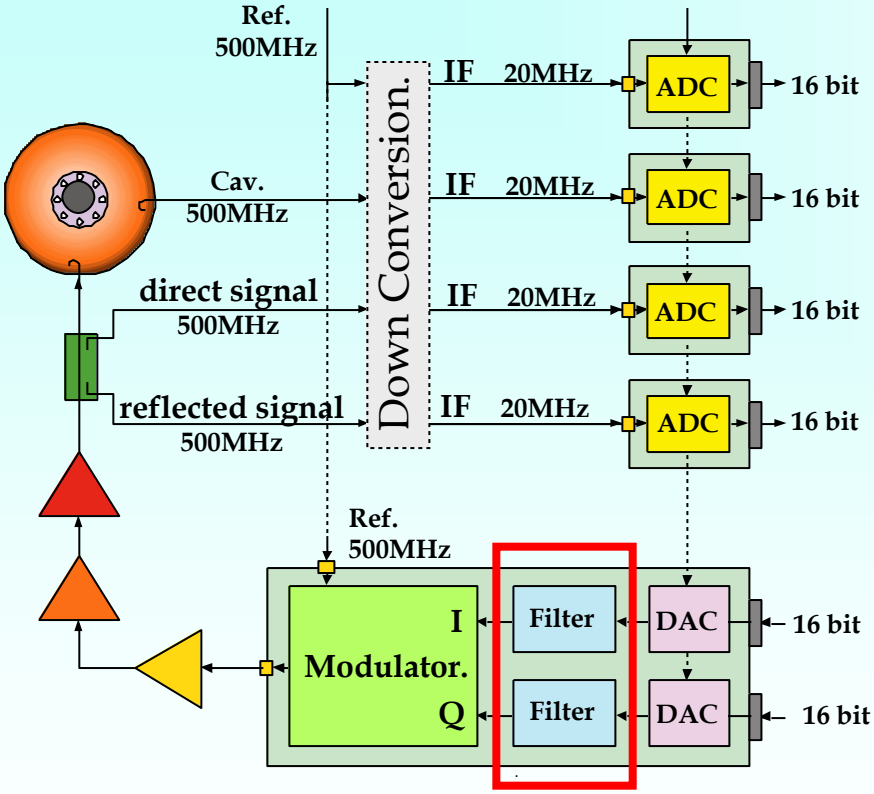


Phase Resolution ±0.1 deg ⇨ 11bit
Amplitude Resolution ± 0.1 % ⇨ 11bit
Clk ⇨ 160MS/s (like ADC)

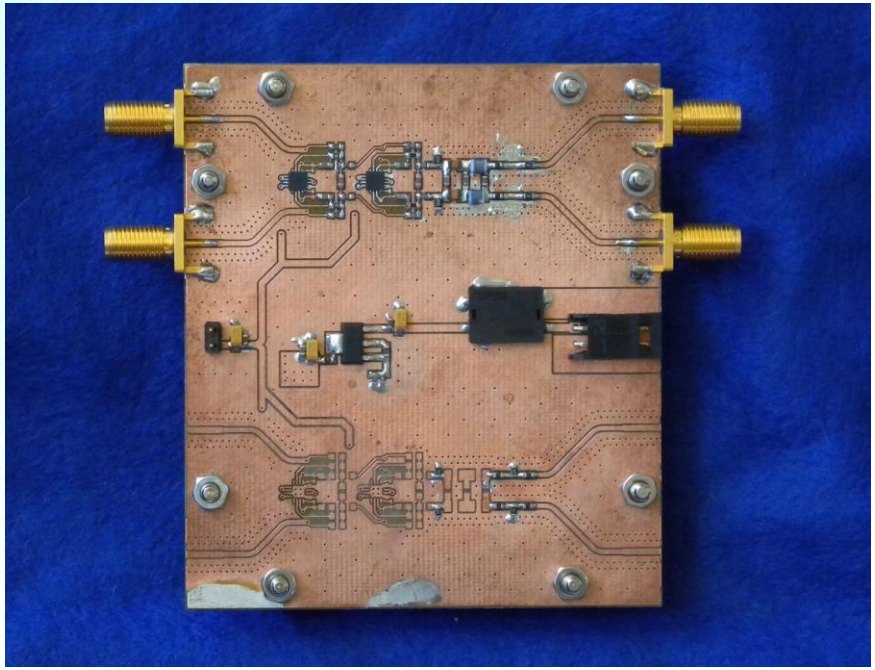
DAC: MAX5891
600 MS/s
16 bit
ENOB = 13 bit



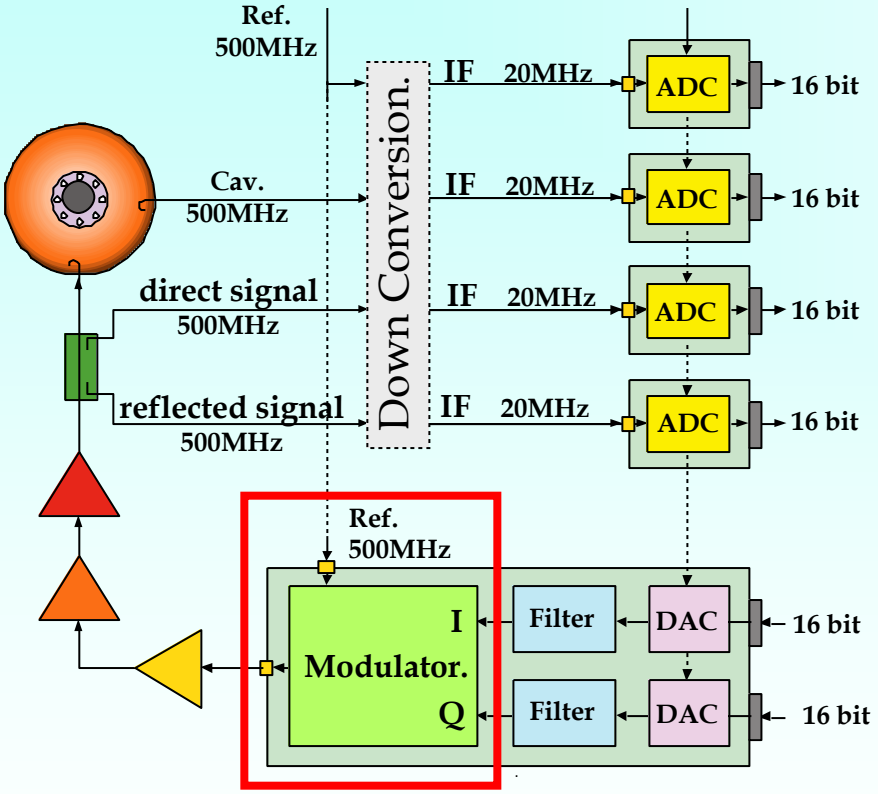
Converters and Modulator - 3



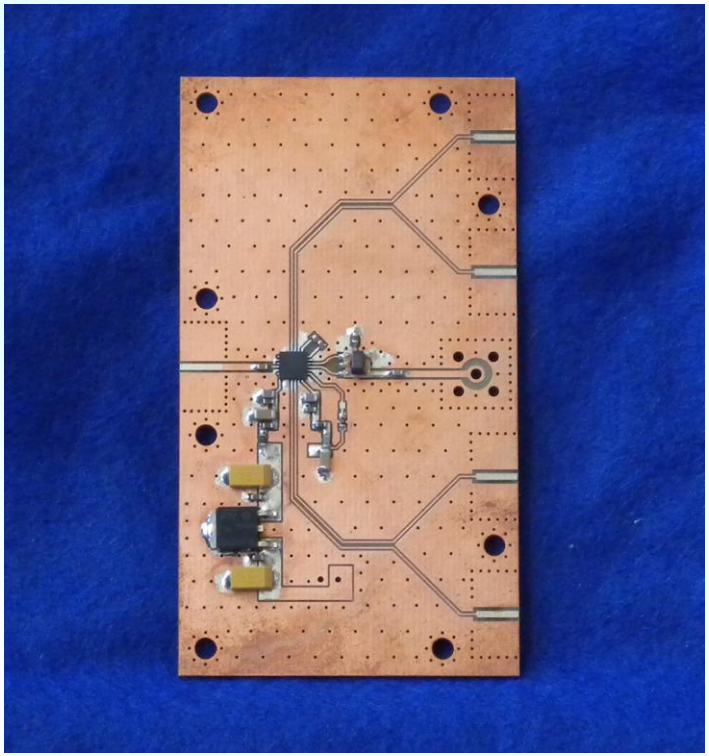
Low Pass Bessel Filter:
Passive filter f_T = 8MHz
Active filter f_T = 150kHz



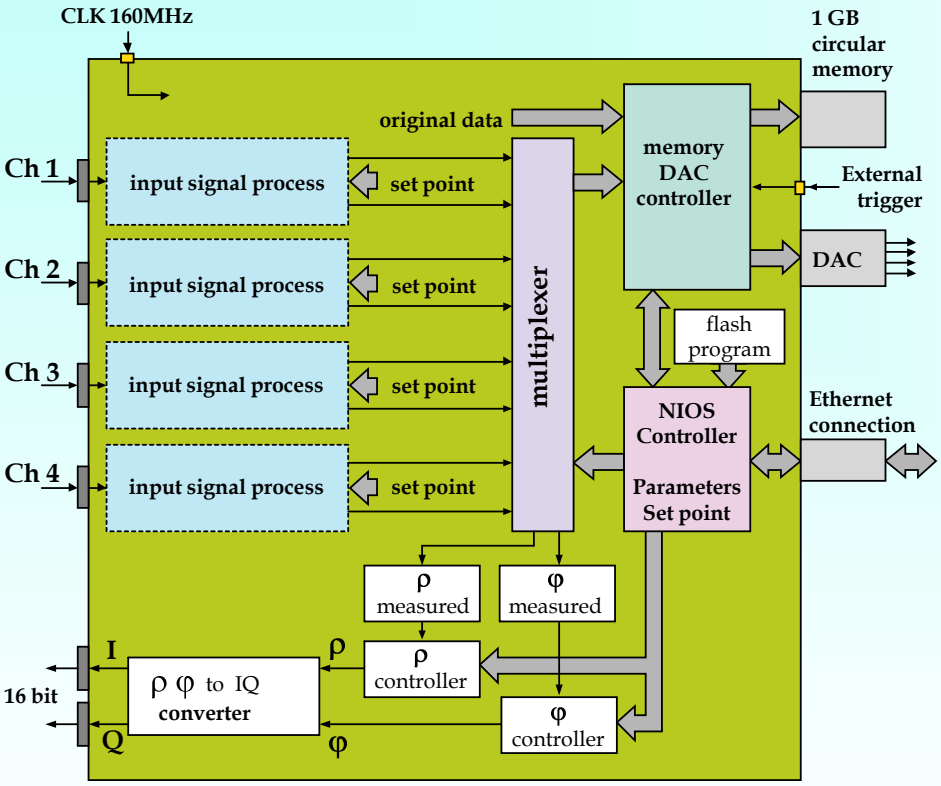
Converters and Modulator - 4

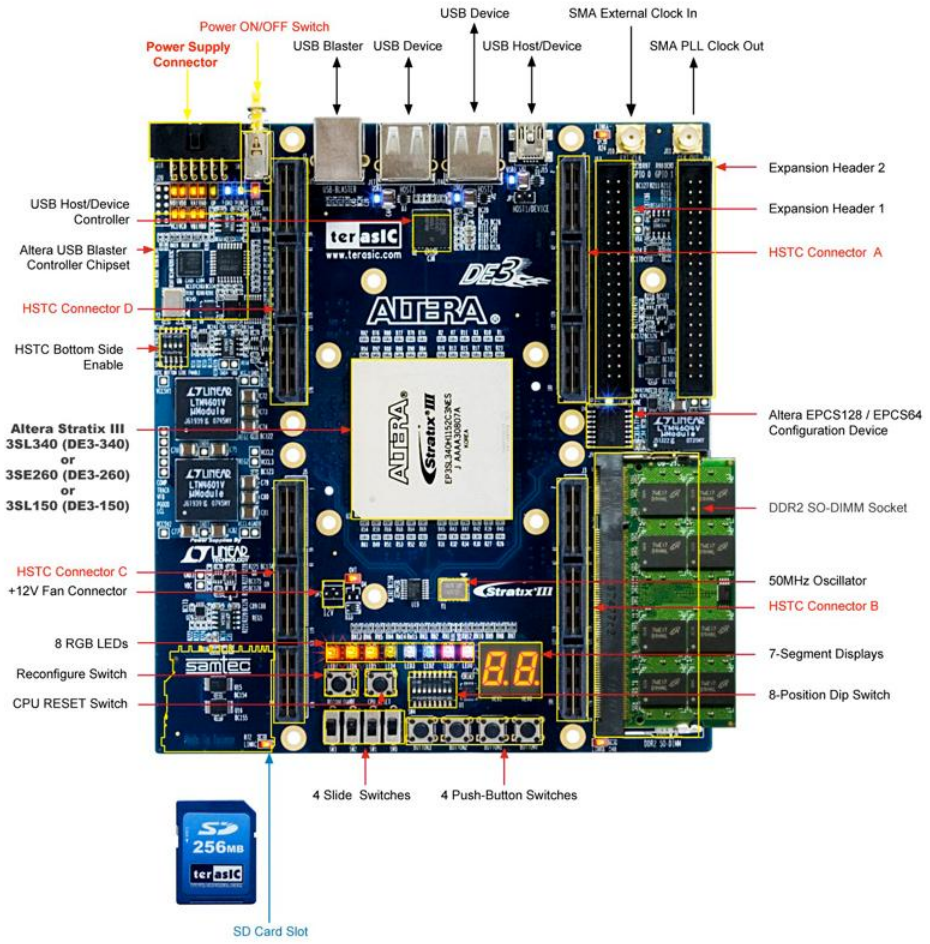


Modulator: LTC5598
RF Range: 5MHz to 1600MHz
Baseband Bandwidth: 400 MHz

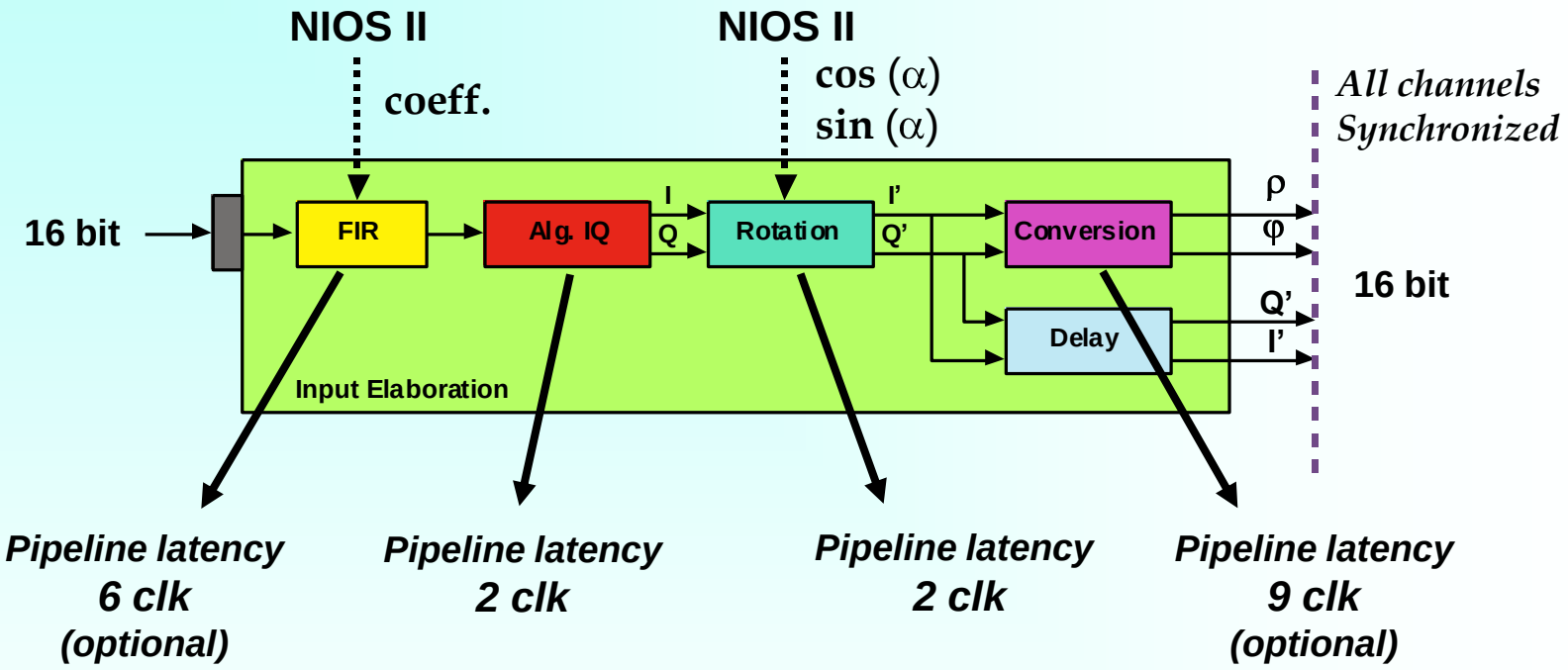


Digital Section - Overview





Digital Section – input signal process



Worst case (whole process): 19 clk (119 ns @ 160MHz)

Digital Section – some detail

		Stratix III L FPGAs (1.1V, 0.9V)					
		EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340
Density and speed	ALMs	19,000	27,000	42,600	56,800	79,560	135,200
	Equivalent LEs	47,500	67,500	107,500	142,500	198,900	338,000
	Registers[1]	38,000	54,000	85,200	113,600	159,120	270,400
	M9K memory blocks	108	150	275	355	468	1,040
	M144K memory blocks	6	6	12	16	36	48
	MLAB memory (Kbits)[2]	297	422	672	891	1,250	2,110
	Embedded memory (Kbits)	1,836	2,214	4,203	5,499	9,396	16,272
	18-bit x 18-bit multipliers	216	288	288	384	576	576
	Speed grades (fastest to slowest)	-2, -3, -4					
Architectural features	Global clock networks	16					
	Regional clock networks	48	48	48	48	88	88
	Periphery clock networks	104	104	208	208	208	208
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96
	Design security	✓					
	Configuration file size (Mbits)	22	22	47	47	66	120
	HardCopy series device support	✓					
	Other	Programmable Power Technology					
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	Emulated LVDS channels, 1,100 Mbps	56	56	88	88	112	137
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132
	Embedded DPA circuitry	✓					
	Series and differential OCT	✓					
	Programmable drive strength	✓					
	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

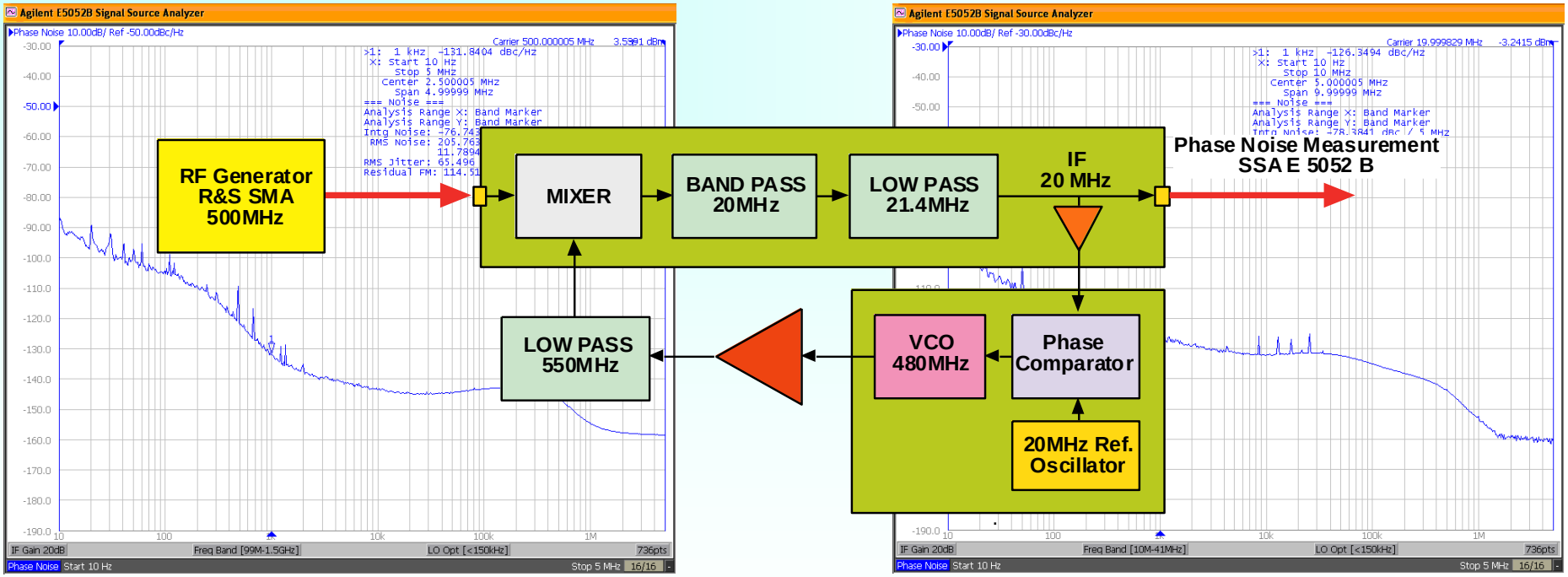
Monitor and control of "high level" operations through the "Nios II" embedded microprocessor

First results:

Noise Measurements with SSA:

Generator @500MHz
RMS Jitter: 11.8 mdeg

IF @20MHz
RMS Jitter: 9.8 mdeg



Final Considerations and next steps

- *First measurements confirm the validity of the architecture: every parameter (Phase, Amplitude) is controlled widely within the requirements*
- *The system actually is "modular", i.e. is compatible with frequencies different from the 500 MHz of Elettra within the range from 40 MHz to 1600 MHz*
- *First tests of ADC section allow us to foresee no appreciable contribution from ADC non linearity*

- *Measurements on bench of RF signal (amplitude and phase shifts) through the complete acquisition chain (RF ⇨ Down Conversion ⇨ ADC sampling) are in progress.*
- *In November the system will be tested with the cavity.*